**Amendments to the Specification:**

Please replace the title with the following new title:

Low Resistance Bandgap Reference Circuit With Resistive T- Network.

Please replace the paragraph beginning on page 9, line 23, and continuing to page 10, line 11, with the following amended paragraph:

Fig. 4 shows the BGR circuit 70 of Fig. 2 in more detail. As can be seen from a comparison of the BGR circuits 10 and 70, the BGR circuit 70 is a modified form of the BGR circuit 10, with the passive resistor T-network 60 of Fig. 3 being added and the individual resistors R1 (42) and R2 (50) in Fig. 1 being eliminated as discussed hereinbefore. All other circuit elements in BGR circuits 10 and 70 remain identical and, therefore, the discussion of various circuit elements and their interconnection given hereinbefore under the "Background" section is not repeated here for the sake of brevity. As mentioned hereinbefore with reference to Fig. 2, the BGR circuit 70 includes a CMOS transistor network 58. The transistor network 58, as can be seen from Fig. 4, includes the three CMOS transistors P1 (14), P2 (16) and P3 (18). The transistor network 58 additionally may also include the diode 44 and N parallel diodes 48, and the resistors R3 (46) and R4 (52). All of the elements in the transistor network 58 are appropriately biased. Also, although not shown in Figs. 1 and 4, it is understood that the op-amp 12 is also connected to appropriate supply and ground potentials. It is noted here that although the BGR circuit 70 is shown to include PMOS transistors, it is known in the art that a similar BGR circuit with appropriately biased NMOS (N-substrate MOS) transistors may also be constructed, instead of the PMOS transistor configuration of Fig. 4. Further, instead of using CMOS transistors 14, 16, 18, the BGR circuit 70 may also be ~~construed~~ constructed using dynamic-threshold MOS transistors (DTMOST), bipolar junction transistors, or BICMOS devices.

Please replace the Abstract with the following amended Abstract:

A CMOS bandgap reference (BGR) voltage generator circuit has a passive resistor T-network of low resistance connected between the inverting and non-inverting inputs of the op-amp in the circuit. The op-amp's output is connected to the gates of three PMOS transistors and the drains of two of the transistors are connected in a looped manner to the input terminals of the

op-amp. The T-network is placed between these drains that connect to the op-amp. ~~The overall resistance in the present circuit is substantially lower than the resistance in the prior art BGR circuit of comparable performance. Hence, the chip area occupied by the resistors in the circuit is substantially reduced when compared with the area occupied by the resistors in the prior art BGR circuit. The circuit provides a steady reference voltage with sub-1V supply and very low power consumption.~~